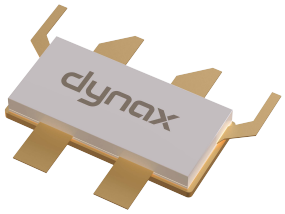
DXG2CH27A-500EFV

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG2CH27A-500EFV is a 500 W RF GaN HEMT Transistor with first generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from 2500 MHz to 2700 MHz.

Table 1. Typical performance [1]

Freq (MHz)	P_{sat} [2] (dBm)	P_{avg} [3] (dBm)	η_D [3] (%)	G_P [3] (dB)	ACPR [3] (dBc)
2496	56.9	47.2	52.6	15.0	-30.0
2593	56.7	47.2	52.9	15.0	-32.9
2690	56.1	47.2	54.7	14.6	-33.6

[1] Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: V_{DS} = 47 V, I_{DQA} = 500 mA, V_{GSB} = - 5.4 V.

[2] Test condition: Input signal Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ±5 MHz offset.

1.2 Features and benefits

- High efficiency, high gain
- Internally matched for broadband performance
- Designed for Digital Pre-Distortion error correction systems
- Optimized for Doherty applications

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 2496 MHz to 2690 MHz frequency range

1.4 Lead-free and RoHS compliant

Pb RoHS

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2. Pinning information

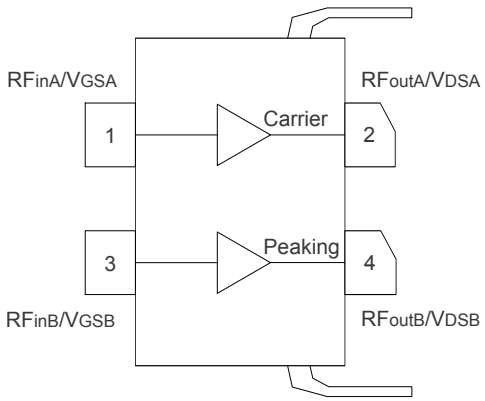

Fig 1. Pin configuration (Top view)

3. Ordering information

Table 2. Ordering information

Part number	Marking	Package type	Packaging information
DXG2CH27A-500EFV	DXG2CH27A-500EFV	780P2LB	Tray: Suffix = 20 units
			Tape and Reel: Suffix = 100 units; 44 mm Tape width; 13-inch Reel

4. Maximum ratings

Table 3. Maximum ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Operating Voltage	V_{DS}	0 ~ +55	V
Maximum Forward Gate Current	I_{GMAX}	59.8	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [1]	T_{MAX}	275	℃

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; Operation beyond T_{MAX} could cause permanent damage.

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5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 50.4 W	R_{thjc}(IR)	1.1	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 50.4 W	R_{thjc}(FEA)	1.5	℃/W
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 12.6 W	R_{thjc}(IR)	0.8	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 12.6 W	R_{thjc}(FEA)	1.1	℃/W

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2012)	1B (≥ 500 V)
Charged Device Model (per JESD22-C101F)	C3 (≥ 1000 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test Methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 1

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8. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	24.6	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 24.6 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 24.6 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 500 mA)	$V_{GS(Q)}$	-	-3.0	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	35.2	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 35.2 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 35.2 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 700 mA)	$V_{GS(Q)}$	-	-3.0	-	V

Table 8. RF characteristics (Typical Doherty performance – 2595 MHz) [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power [2]	P_{sat}	55.6	56.6	-	dBm
Drain Efficiency [3]	η_D	44.0	51.0	-	%
Power Gain [3]	G_P	14.4	16.0	17.6	dB

[1] Typical Doherty performance in Dynax DXG2CH27A-500EFV production test fixture, test condition: V_{DS} = 52 V, I_{DQA} = 320 mA, V_{GSB} = -1.95 V + V_{GSQ} @320 mA.

[2] Test condition: Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: P_{avg} = 48.5 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.2 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V_{DS} = 52 V, 500 W Pulsed CW output power, Pulse width = 100 µs, Duty cycle = 10%.	No device damage

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9. Test information

9.1 Typical application circuit

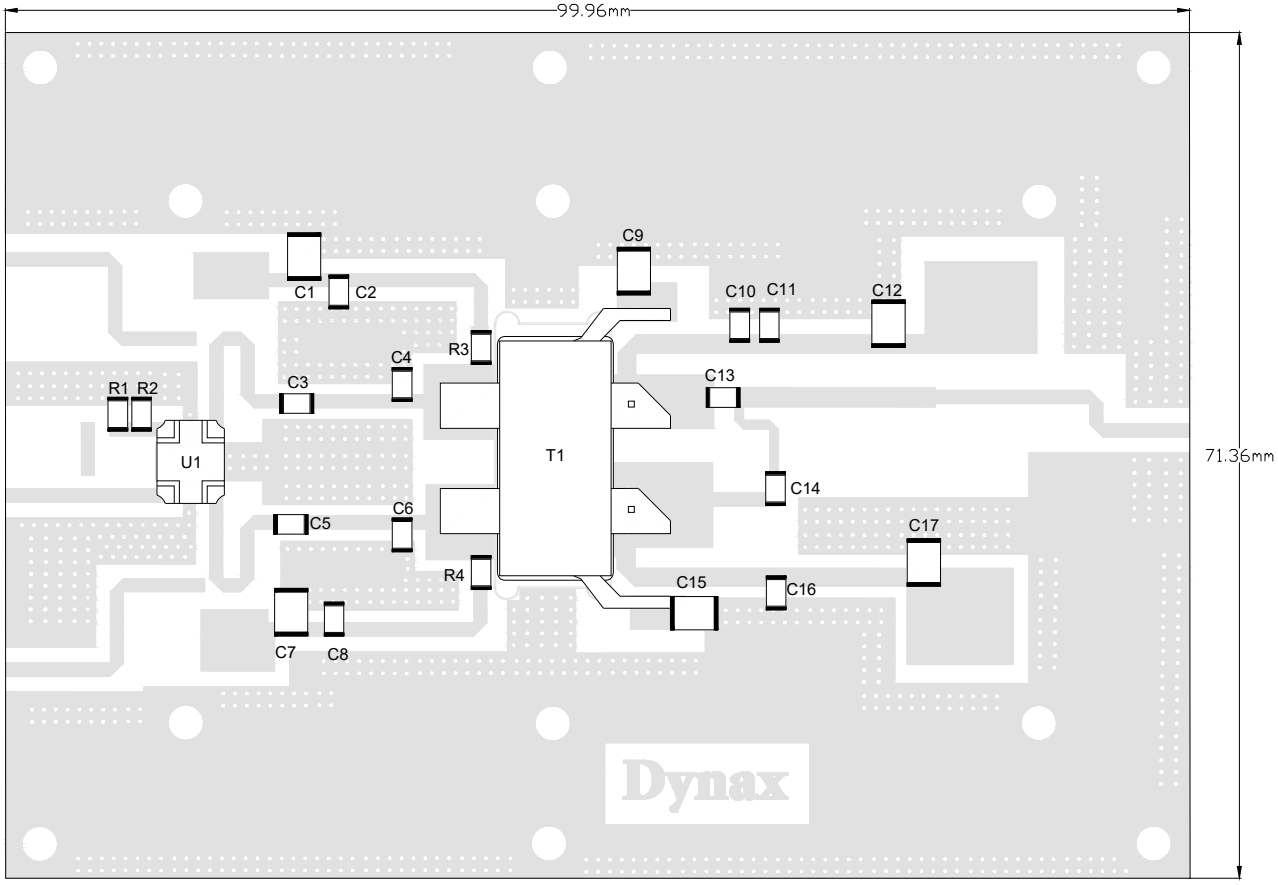

Fig 2. Component layout

Table 10. List of components

S/N	Type	Designator	Description	Value	Vendor
1	Cap	C2,C3,C5,C8,C10,C11,C14,C16	ATC600F9R1JT250XT	9.1 pF	ATC
2	Cap	C13	ATC600F3R6JT250XT	3.6 pF	ATC
3	Cap	C1,C7,C9,C12,C15,C17	GRM32DC72A225KE01L	2.2 uF	Murata
4	Cap	C4	ATC600F1R2JT250XT	1.2 pF	ATC
5	Cap	C6	ATC600F1R5JT250XT	1.5 pF	ATC
6	Res	R3,R4	RC0805FR_0710RL	10 Ω	Yageo
7	Res	R1,R2	RC0805FR_07100RL	100 Ω	Yageo
8	Hybrid Coupler	U1	X3C26P1-03S	3 dB	Anaren
9	Transistor	T1	DXG2CH27A-500EFV	/	Transistor
10	PCB	/	Ro4350B	20 mil	PCB

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9.2 Graphic data

9.2.1 Pulsed CW

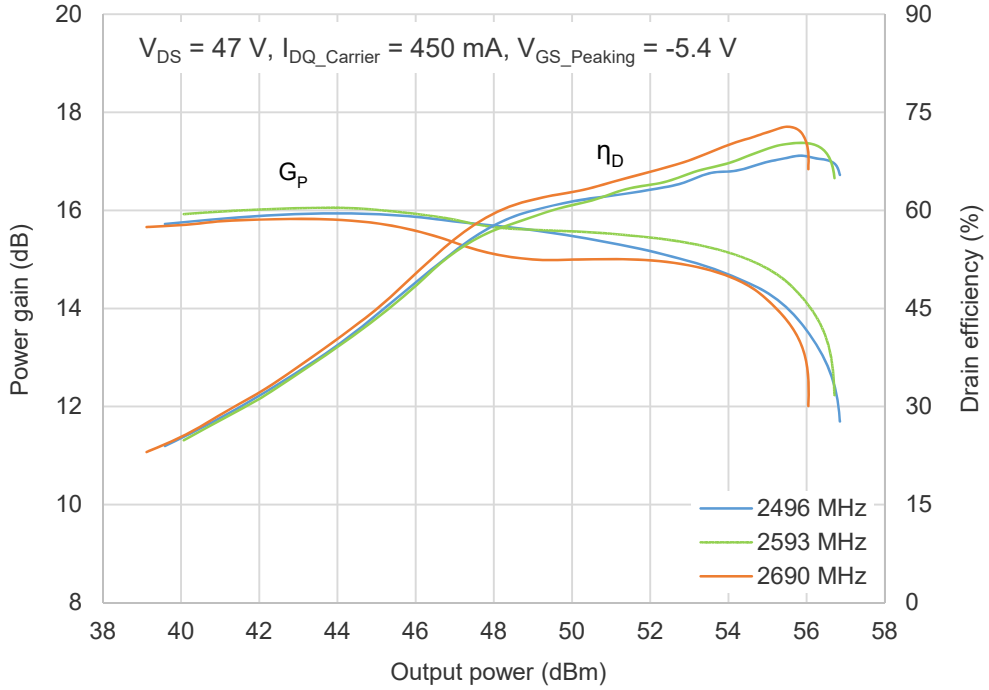

Fig 3. Power gain, Drain efficiency vs. Pulse output power

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10. Impedance information

Table 11. Typical impedance of carrier [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	3.4 - j8.8	5.7 - j13.2	18.5	54.0	251	69.8
2700	7.5 - j7.8	5.4 - j14.0	18.5	53.9	245	69.0
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	3.4 - j8.8	9.6 - j4.9	20.2	51.3	135	79.8
2700	7.5 - j7.8	6.3 - j7.8	20.0	51.6	145	80.5

Table 12. Typical impedance of peaking [2]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	6.0 - j6.5	3.0 - j12.0	18.2	55.2	331	65.4
2700	5.3 - j2.0	3.1 - j13.1	18.2	55.1	324	64.6
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	6.0 - j6.5	4.9 - j7.5	19.8	52.4	174	78.5
2700	5.3 - j2.0	3.0 - j8.9	20.2	51.9	155	77.5

[1] V_{DS} = 48 V, I_{DQA} = 500 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[2] V_{DS} = 48 V, I_{DQB} = 700 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

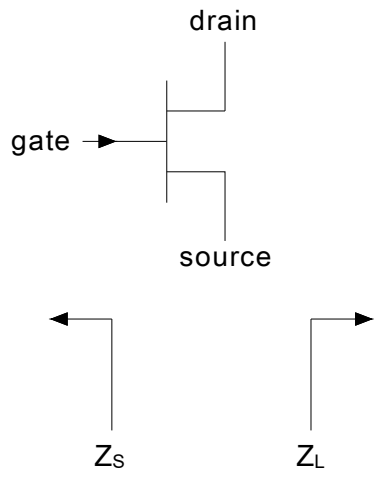

Fig 4. Definition of transistor impedance

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11. Median lifetime

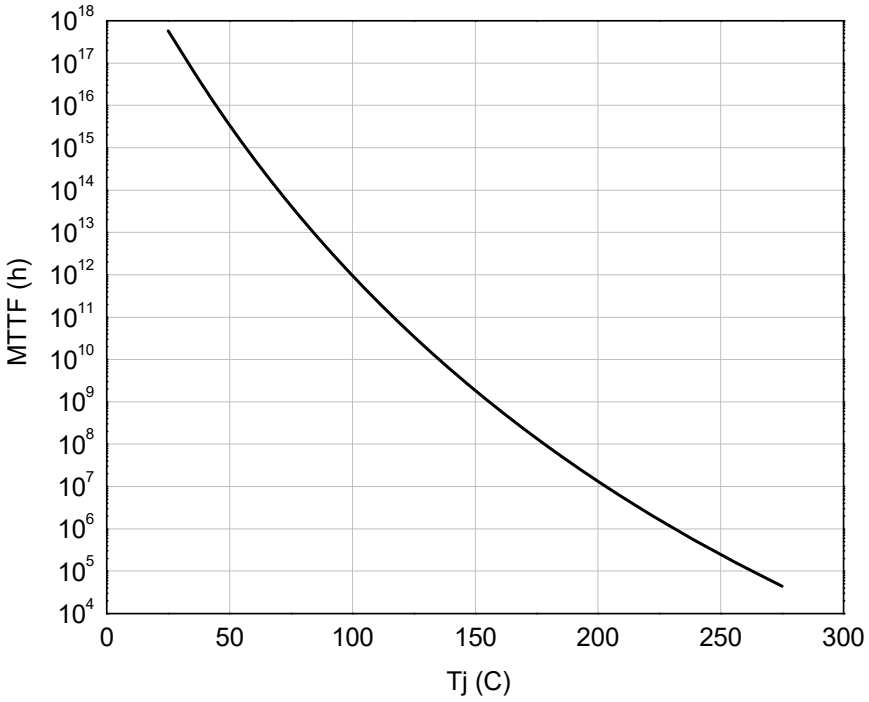

Fig 5. Median lifetime vs. channel temperature

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12. Package outline

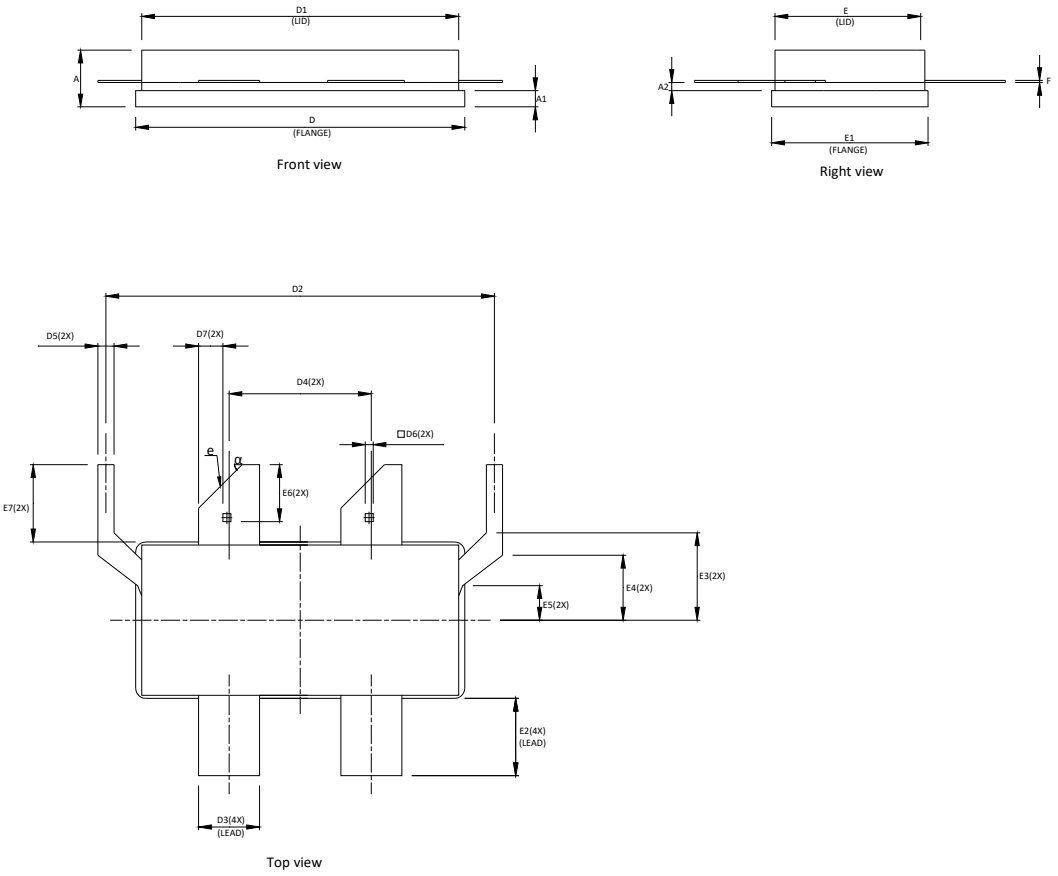

Fig 6. Package outline —— 780P2LB

Table 13. Package dimensions

DIM	INCH			MILLIMETER		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.129	0.142	0.156	3.27	3.61	3.95
A1	0.037	0.040	0.043	0.95	1.02	1.09
A2	0.017	0.020	0.023	0.44	0.51	0.58
D	0.807	0.810	0.813	20.51	20.58	20.65
D1	0.772	0.780	0.788	19.61	19.82	20.02
D2	0.951	0.956	0.961	24.16	24.28	24.40
D3	0.145	0.150	0.155	3.69	3.81	3.93
D4	0.345	0.350	0.355	8.77	8.89	9.01
D5	0.035	0.040	0.044	0.89	1.01	1.13
D6	0.018	0.020	0.022	0.45	0.50	0.55
D7	0.058	0.060	0.062	1.47	1.52	1.57

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(Continued)

E	0.365	0.370	0.375	9.27	9.40	9.53
E1	0.382	0.385	0.388	9.71	9.78	9.85
E2	0.181	0.190	0.198	4.61	4.83	5.04
E3	0.210	0.215	0.220	5.34	5.46	5.58
E4	0.155	0.160	0.165	3.94	4.06	4.18
E5	0.080	0.085	0.090	2.04	2.16	2.28
E6	0.138	0.140	0.142	3.50	3.55	3.60
E7	0.181	0.190	0.198	4.61	4.83	5.04
F	0.003	0.005	0.006	0.08	0.12	0.15
e	TYP 0.107			TYP 2.72		
α	45° REF			45° REF		

13. Abbreviations

Table 14. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
Production [short] datasheet	Mass product	This document contains the product specification.

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