5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 8.0 W	R_{thjc}(IR)	4.2	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 8.0 W	R_{thjc}(FEA)	6.4	℃/W
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 2.0 W	R_{thjc}(IR)	2.5	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 2.0 W	R_{thjc}(FEA)	4.8	℃/W

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2012)	1A (≥ 250 V)
Charged Device Model (per JESD22-C101F)	C2 (≥ 500 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test Methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 3

8. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	4.0	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 4.0 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 4.0 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 90 mA)	$V_{GS(Q)}$	-	-3.0	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	5.4	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 5.4 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 5.4 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 120 mA)	$V_{GS(Q)}$	-	-3.0	-	V

Table 8. RF characteristics (Typical Doherty performance – 2700 MHz) [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power [2]	P_{sat}	47.1	48.1	-	dBm
Drain Efficiency [3]	η_D	44.8	51.8	-	%
Power Gain [3]	G_P	13.9	15.5	17.1	dB

[1] Typical Doherty performance in Dynax DXG2PH27A-100N production test fixture, test condition: V_{DS} = 48 V, I_{DQA} = 90mA, V_{GSB} = -2.9 V + V_{GSQ} @15 mA.

[2] Test condition: Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: P_{avg} = 41.3 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V_{DS} = 48 V, 100 W Pulsed CW output power, Pulse width = 100 µs, Duty cycle = 10%.	No device damage

9. Test information

9.1 Typical application circuit

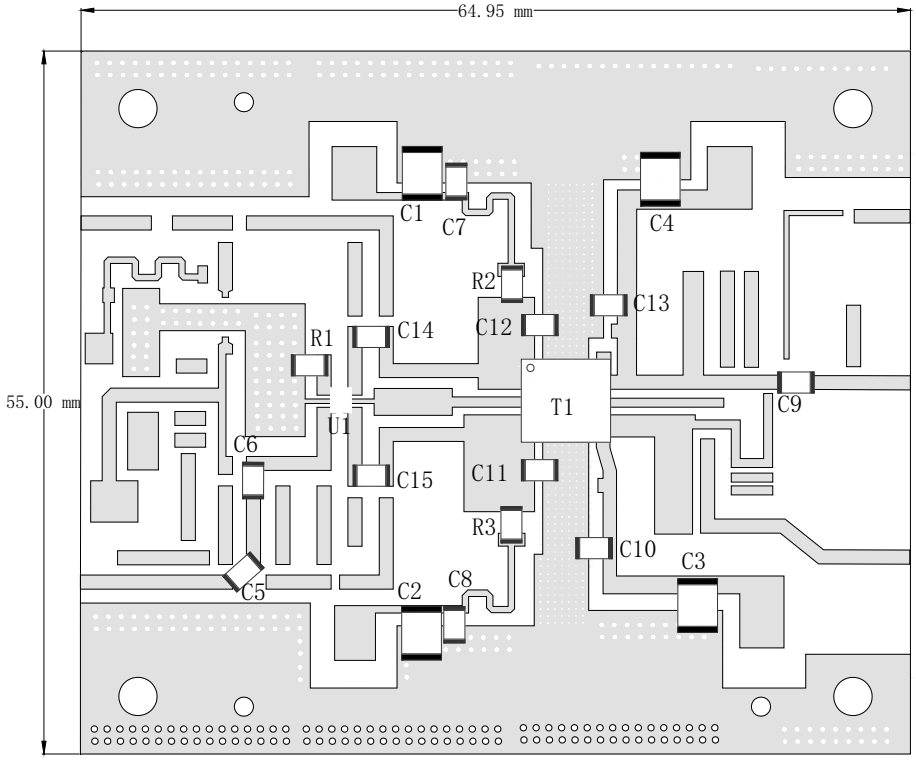

Fig 2. Component layout

Table 10. List of components

S/N	Type	Designator	Description	Value	Vendor
1	Cap	C1,C2,C3,C4	GRM32ER72A225KA	2.2 uF	Murata
2	Cap	C5,C6,C7,C8,C9,C10,C13,C14,C15	ATC600F10R0JT250XT	10pF	ATC
3	Cap	C11	ATC600F1R0JT250XT	1.0pF	ATC
4	Cap	C12	ATC600F0R7JT250XT	0.7pF	ATC
5	Res	R1	RC0805FR_0750RL	50Ω	Yageo
6	Res	R2,R3	RC0805FR_0710RL	10Ω	Yageo
7	Hybrid Coupler	U1	C3337J5003AHF	3dB	Anaren
8	Transistor	T1	DXG2PH27A-100N	/	Dynax
9	PCB	/	Rogers 4350B	20 mil	Rogers

9.2 Graphic data

9.2.1 Pulsed CW

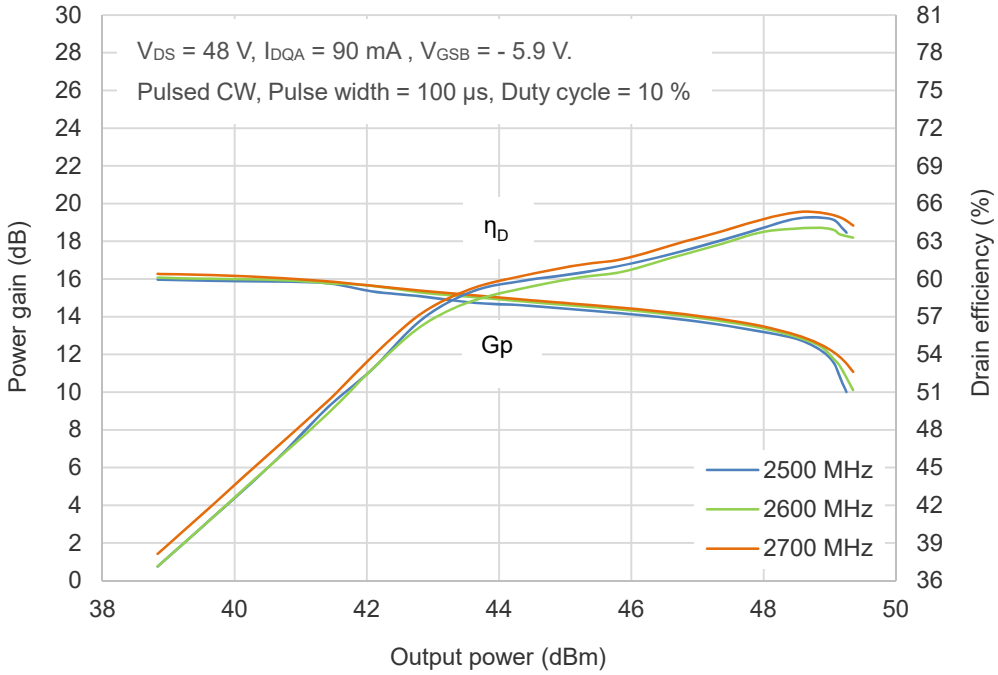

Fig 3. Power gain, Drain efficiency vs. Pulse output power

10. Impedance information

10.1 Impedance information

Table 11. Typical impedance of carrier [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	6.9 - j14.5	10.5 + j2.9	20.3	46.7	47.0	69.2
2600	10.8 - j15.7	9.8 + j2.8	20.3	46.7	47.0	69.5
2700	13.7 - j18.8	9.1 + j2.1	20.4	46.6	46.0	70.0
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	6.9 - j14.5	6.9 + j12.8	21.9	43.9	25.0	82.4
2600	10.8 - j15.7	6.5 + j11.5	21.8	43.8	24.0	82.6
2700	13.7 - j18.8	6.0 + j10.5	21.7	43.7	23.0	83.0

Table 12. Typical impedance of peaking [2]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	5.6 - j15.2	11.8 + j1.5	21.2	48.2	66.0	64.2
2600	9.8 - j19.8	11.2 + j0.8	21.1	48.2	66.0	64.0
2700	17.6 - j25.2	10.7 + j0.1	20.8	48.1	65.0	63.5
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2500	5.6 - j15.2	5.0 + j9.0	23.1	46.3	43.0	75.0
2600	9.8 - j19.8	6.5 + j7.8	22.8	46.2	42.0	74.2
2700	17.6 - j25.2	5.2 + j5.2	22.6	46.0	40.0	74.5

[1] V_{DS} = 48 V, I_{DQA} = 90 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[2] V_{DS} = 48 V, I_{DQB} = 120 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

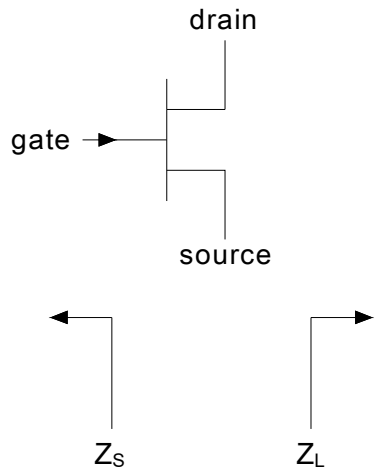

Fig 4. Definition of transistor impedance

11. Median lifetime

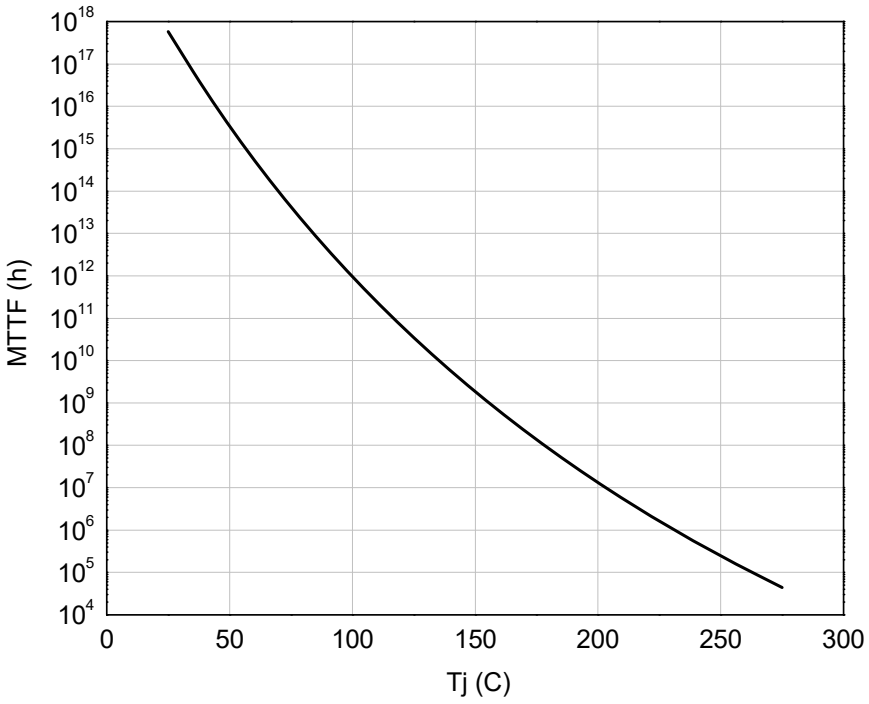

Fig 5. Median lifetime vs. channel temperature

12. Package outline

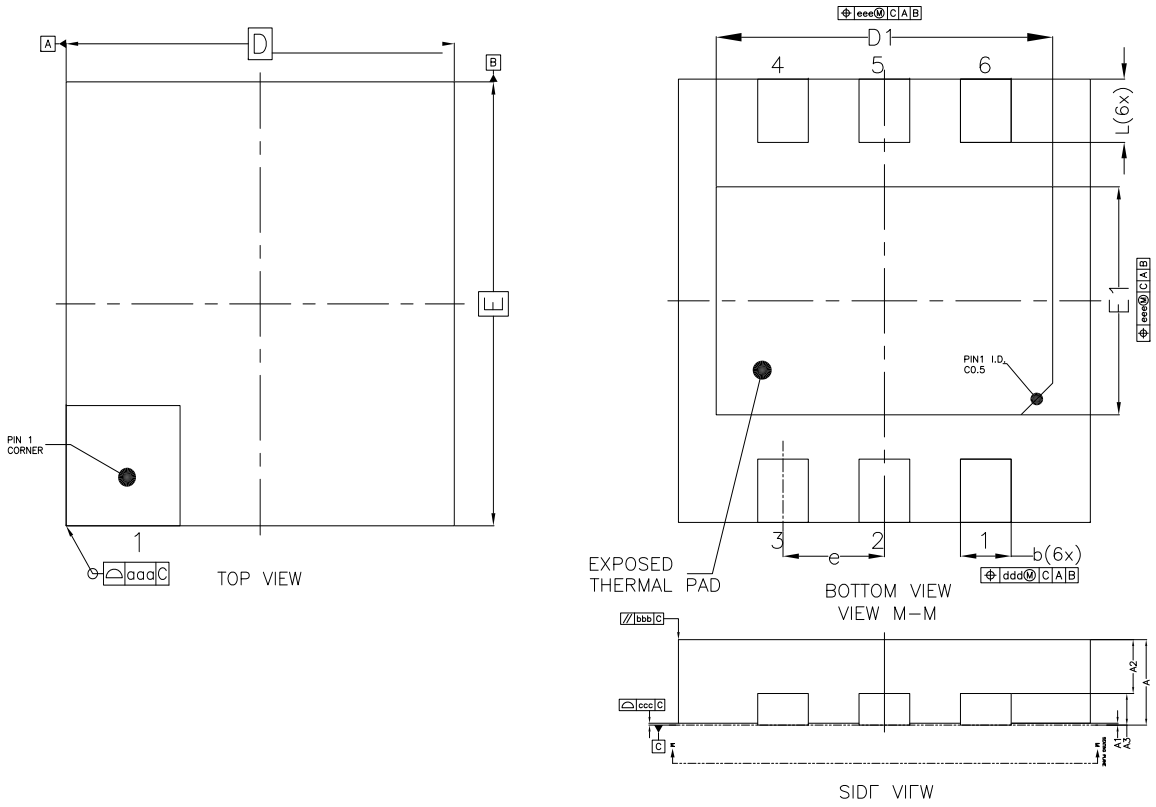

Fig 6. Package outline —— DFN 7×6.5mm

Table 13. Package dimensions

DESCRIPTION		DIM	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	1.30	1.35	1.40
STAND OFF		A1	0.00	-----	0.05
MOLD THICKNESS		A2	0.80	0.85	0.90
L/F THICKNESS		A3	0.50 REF		
BODY SIZE	X	D	6.43	6.50	6.57
	Y	E	6.93	7.00	7.07
LEAD PITCH		e	1.60 BSC		
LEAD WIDTH		b	0.75	0.80	0.85
LEAD LENGTH		L	0.95	1.00	1.05
EP SIZE		D1	5.26	5.31	5.36
		E1	3.55	3.60	3.65
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

13. Abbreviations

Table 14. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
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