

5. Thermal characteristics

Table 4. Thermal characteristics

| Parameter | Symbol | Value | Unit |
|---|-------------------------------|-------|----------------------|
| Side A, Carrier | | | |
| Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 6.3 \text{ W}$ | $R_{\text{thjc}}(\text{IR})$ | 5.8 | $^{\circ}\text{C/W}$ |
| Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 6.3 \text{ W}$ | $R_{\text{thjc}}(\text{FEA})$ | 9.3 | $^{\circ}\text{C/W}$ |
| Side B, Peaking | | | |
| Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 1.5 \text{ W}$ | $R_{\text{thjc}}(\text{IR})$ | 7.1 | $^{\circ}\text{C/W}$ |
| Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 1.5 \text{ W}$ | $R_{\text{thjc}}(\text{FEA})$ | 9.7 | $^{\circ}\text{C/W}$ |

6. ESD protection characteristics

Table 5. ESD protection characteristics

| Test Methodology | Class |
|---|---------------|
| Human Body Model (per JS-001-2012) | 1A (> 250 V) |
| Charged Device Model (per JESD22-C101F) | C3 (> 1000 V) |

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

| Test Methodology | Class |
|--|---------|
| Moisture Sensitivity Level (per J-STD-020) | Level 3 |

8. Electrical characteristics (TA = 25°C unless otherwise noted)

Table 7. DC characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|----------------------|------|------|------|------|
| Side A, Carrier | | | | | |
| Drain-Source Leakage Current (V _{GS} = -10 V, V _{DS} = 150 V) | I _{DSS} | - | - | 2.5 | mA |
| Drain-Source Breakdown Voltage (V _{GS} = -10 V, I _D = 2.5 mA) | V _{(BR)DSS} | 150 | - | - | V |
| Gate Threshold Voltage (V _{DS} = 48 V, I _D = 2.5 mA) | V _{GS(th)} | -4.0 | -3.3 | -1.0 | V |
| Gate Quiescent Voltage (V _{DS} = 48 V, I _D = 100 mA) | V _{GS(Q)} | - | -3.1 | - | V |
| Side B, Peaking | | | | | |
| Drain-Source Leakage Current (V _{GS} = -10 V, V _{DS} = 150 V) | I _{DSS} | - | - | 3.9 | mA |
| Drain-Source Breakdown Voltage (V _{GS} = -10 V, I _D = 3.9 mA) | V _{(BR)DSS} | 150 | - | - | V |
| Gate Threshold Voltage (V _{DS} = 48 V, I _D = 3.9 mA) | V _{GS(th)} | -4.0 | -3.3 | -1.0 | V |
| Gate Quiescent Voltage (V _{DS} = 48 V, I _D = 150 mA) | V _{GS(Q)} | - | -3.1 | - | V |

Table 8. RF characteristics (Typical Doherty performance – 3700 MHz) ¹

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------|------|------|------|------|
| Peak Output Power ² | P _{sat} | 45.9 | 46.9 | - | dBm |
| Drain Efficiency ³ | η _D | 46.3 | 53.3 | - | % |
| Power Gain ³ | G _P | 12.3 | 13.9 | 15.5 | dB |

¹ Typical Doherty performance in Dynax DXG2PH36A-70N production test fixture, test condition: V_{DS} = 48 V, I_{DQA} = 60 mA, V_{GSB} = -2.5 V + V_{GSQ} @15 mA.

² Test condition: Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

³ Test condition: P_{avg} = 39.8 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

| Parameter | Result |
|---|------------------|
| VSWR 10:1 at V _{DS} = 48 V, 70 W Pulsed CW output power, Pulse width = 100 μs, Duty cycle = 10%. | No device damage |

9.2 Graphic data

9.2.1 Pulsed CW

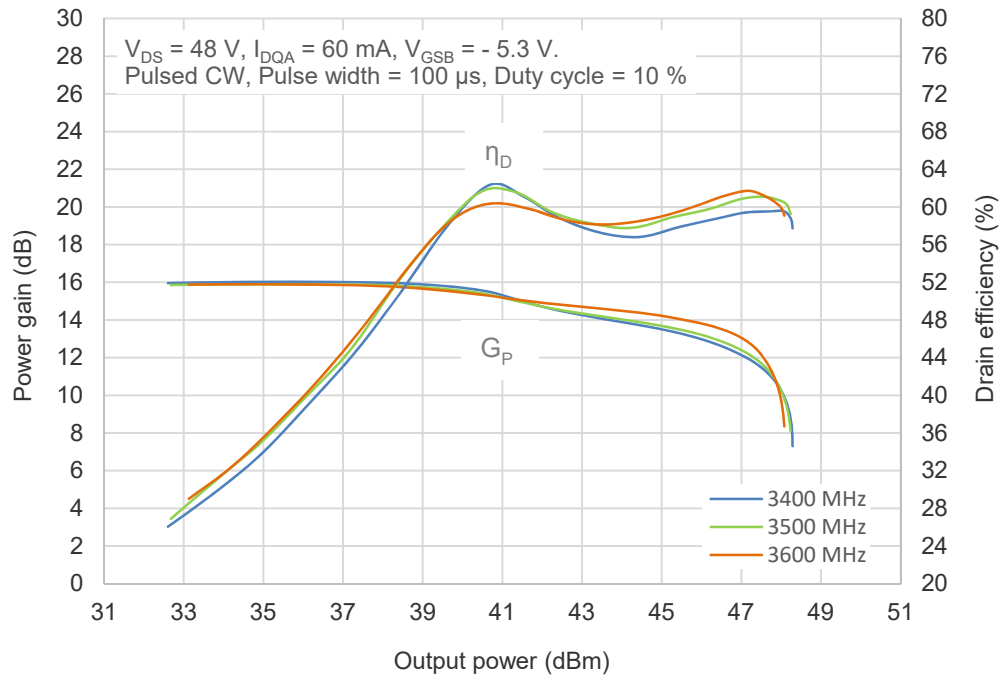


Fig 3. Power gain, Drain efficiency vs. Pulse output power

10. Impedance information

10.1 Impedance information

Table 11. Typical impedance of carrier ¹

| Maximum Output Power | | | | | | |
|--------------------------|--------------------|--------------------|---------------------|------------------------|----------------------|--------------------|
| Freq (MHz) | Z _S (Ω) | Z _L (Ω) | G _P (dB) | P _{sat} (dBm) | P _{sat} (W) | η _D (%) |
| 3400 | 9.3 - j22.1 | 15.0 + j3.0 | 19.6 | 44.7 | 29.5 | 69.4 |
| 3600 | 14.9 - j24.0 | 14.0 + j1.8 | 19.6 | 44.7 | 29.5 | 69.5 |
| Maximum Drain Efficiency | | | | | | |
| Freq (MHz) | Z _S (Ω) | Z _L (Ω) | G _P (dB) | P _{sat} (dBm) | P _{sat} (W) | η _D (%) |
| 3400 | 9.3 - j22.1 | 6.6 + j14.1 | 22.8 | 41.7 | 14.7 | 81.0 |
| 3600 | 14.9 - j24.0 | 6.5 + j11.2 | 22.4 | 41.9 | 15.4 | 81.3 |

Table 12. Typical impedance of peaking ²

| Maximum Output Power | | | | | | |
|--------------------------|--------------------|--------------------|---------------------|------------------------|----------------------|--------------------|
| Freq (MHz) | Z _S (Ω) | Z _L (Ω) | G _P (dB) | P _{sat} (dBm) | P _{sat} (W) | η _D (%) |
| 3400 | 10.2 - j29.9 | 9.0 - j0.3 | 21.4 | 46.0 | 39.8 | 70.2 |
| 3600 | 20.0 - j26.0 | 7.3 - j1.6 | 22.4 | 45.9 | 38.9 | 71.1 |
| Maximum Drain Efficiency | | | | | | |
| Freq (MHz) | Z _S (Ω) | Z _L (Ω) | G _P (dB) | P _{sat} (dBm) | P _{sat} (W) | η _D (%) |
| 3400 | 10.2 - j29.9 | 6.6 + j5.8 | 23.5 | 44.2 | 26.3 | 80.5 |
| 3600 | 20.0 - j26.0 | 5.7 + j4.5 | 23.3 | 43.8 | 24.0 | 81.0 |

¹ V_{DS} = 48 V, I_{DQA} = 60 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

² V_{DS} = 48 V, I_{DQB} = 100 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

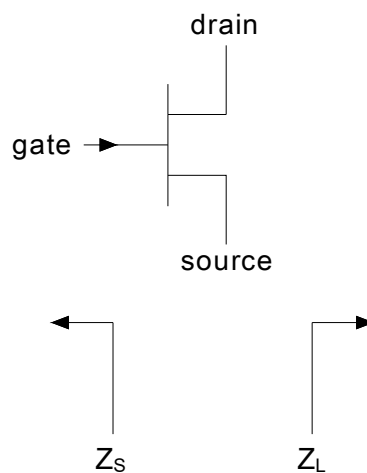


Fig 4. Definition of transistor impedance

11. Median lifetime

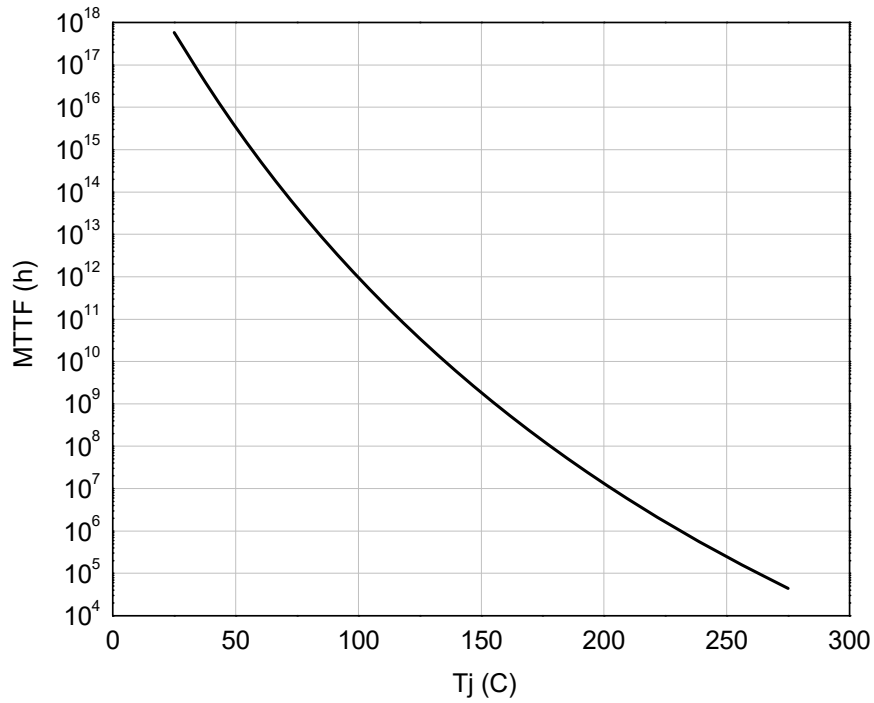


Fig 13. Median lifetime vs. channel temperature

12. Package outline

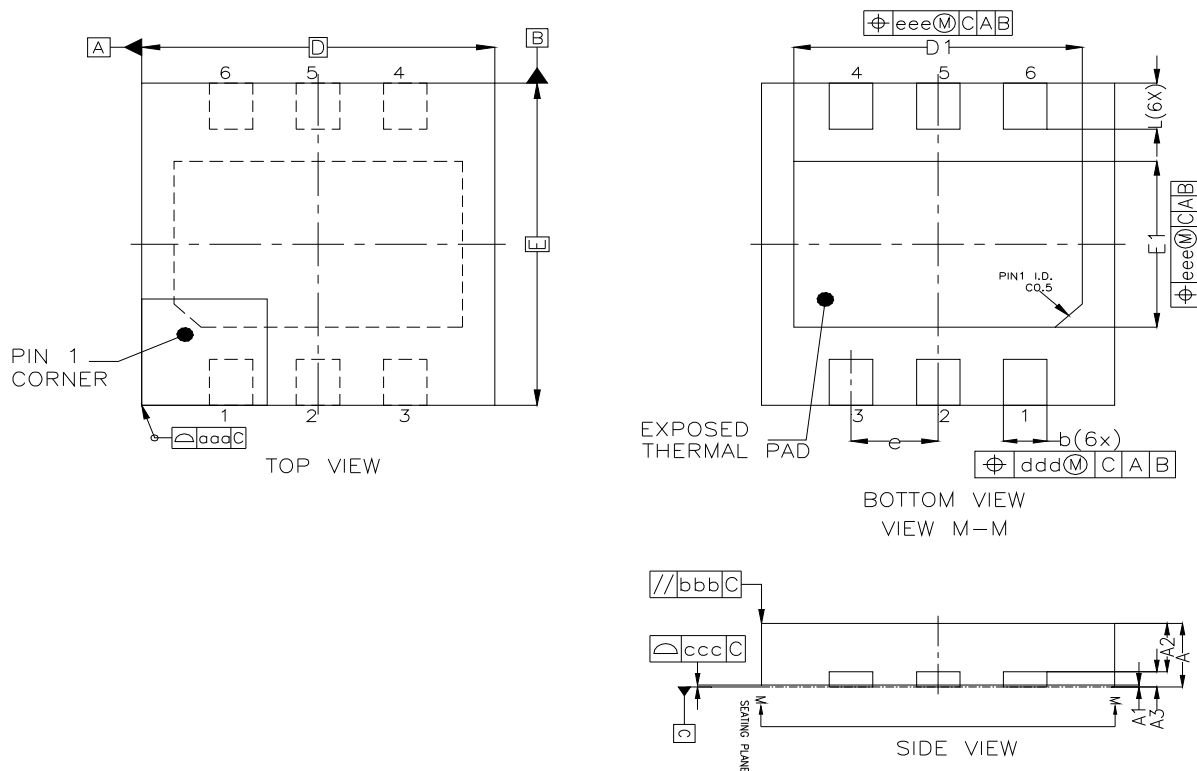


Fig 14. Package outline —DFN 7×6.5mm

Table 13. Package dimensions

| DESCRIPTION | DIM | MILLIMETER | | | |
|--------------------------------|-----|------------|-------|------|------|
| | | MIN | NOM | MAX | |
| TOTAL THICKNESS | A | 0.80 | 0.85 | 0.90 | |
| STAND OFF | A1 | 0.00 | ----- | 0.05 | |
| MOLD THICKNESS | A2 | 0.60 | 0.65 | 0.70 | |
| L/F THICKNESS | A3 | 0.203 REF | | | |
| BODY SIZE | X | D | 6.43 | 6.50 | 6.57 |
| | Y | E | 6.93 | 7.00 | 7.07 |
| LEAD PITCH | e | 1.60 BSC | | | |
| LEAD WIDTH | b | 0.75 | 0.80 | 0.85 | |
| LEAD LENGTH | L | 0.95 | 1.00 | 1.05 | |
| EP SIZE | D1 | 5.26 | 5.31 | 5.36 | |
| | E1 | 3.55 | 3.60 | 3.65 | |
| Tolerance of form and position | | | | | |
| PACKAGE EDGE TOLERANCE | aaa | 0.1 | | | |
| MOLD FLATNESS | bbb | 0.1 | | | |
| LEAD COPLANARITY | ccc | 0.08 | | | |
| LEAD POSITION OFFSET | ddd | 0.1 | | | |
| EXPOSED PAD OFFSET | eee | 0.1 | | | |

13. Abbreviations

Table 14. Abbreviations

| Acronym | Description |
|---------|-----------------------------------|
| CW | Continuous Waveform |
| ESD | Electro-Static Discharge |
| GaN | Gallium Nitride |
| HEMT | High Electron Mobility Transistor |
| MTTF | Median Time To Failure |
| VSWR | Voltage Standing Wave Ratio |

14. Legal information

14.1 Datasheet status

| Document status | Product status | Definition |
|-------------------------------|--------------------|---|
| Objective [short] datasheet | Engineering sample | This document contains data from the objective specification for product development. |
| Preliminary [short] datasheet | Engineering sample | This document contains data from the preliminary specification. |
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